UNITED STATES PATENT AND TRADEMARK OFFICE

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EXAMINER
TABONE JR, JOHN J

ART UNIT	PAPER NUMBER
2117	

NOTIFICATION DATE	DELIVERY MODE
10/16/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2008*.
2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.
    4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) *1-8* is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.
10)☒ The drawing(s) filed on *15 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a)☐ All   b)☐ Some * c)☐ None of:
      1.☐ Certified copies of the priority documents have been received.
      2.☐ Certified copies of the priority documents have been received in Application No. _____.
      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .
5)☐ Notice of Informal Patent Application
6)☐ Other: _____ .

FINAL DETAILED ACTION

1.   Claims 1-8 remain pending in the application and have been examined. Claims 9,

12 and 14-15 have been cancelled.

Response to Arguments

2.   Applicant's arguments with respect to independent claim 1 have been considered

but are moot in view of the new ground(s) of rejection.

As per arguments for independent claim 1:

The Applicants argue, "Shen does not disclose the network server of claim 1.

The debugger workstation of Shen is directly connected with the chip using an I/0 pin

and a bus (3:22-30 and 5:20)". The Examiner disagrees and asserts that the claimed

network server, which is disclosed as debugger server 200, is physically connected to

the debug client 120 as shown in Fig. 3 in a similar manner as Shen.

The Applicants further argue, "the media access controller of claim 1 provides

integrated support for a remotely located network server". The Examiner would like to

point out that nowhere does the disclosure suggest the argued remotely located

network server. The debugger server 200 is physically connected to the debug client

120 and is not remotely located at all.

It is the Examiner's conclusion that independent claim 1 is not patentably distinct

or non-obvious over the prior arts of record namely, Shen et al. (US-6829751).

Therefore, the rejection is maintained. Based on their dependency on independent

claim 1, claims 2-8 stand rejected.

Specification

3.   The disclosure is objected to because of the following informalities: On page 7 of

the specification reference number 240 is used to represent the debug system and the

debugger server. It is not clear to the Examiner what is correct. However, in Fig. 3 the

debug system has the reference number 240 and the debugger server has the

reference number 200.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.-

4.   Claims 1-8 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply

with the enablement requirement. The claim(s) contains subject matter which was not

described in the specification in such a way as to enable one skilled in the art to which it

pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 1:

Even though the media access controller (MAC) 102 is disclosed in the

specification on page 4, lines 13-22, it is not included in the debug client function 120 as

claimed, but located on standard cell design 100. Further, it is the debug client function

120 that receives the debugging session information downloaded from the debugger

server 200, not the MAC 102. (See p. 7, ll. 1-15). Nowhere in the disclosure does the

MAC 102 down-loads information for a debugging session. Therefore, this limitation is

not described in such a way as to enable one skilled in the art to which it pertains, or

with which it is most nearly connected, to make and/or use the invention.

As such the limitation "media access controller to provide communication with the

network server over a network, including downloading information for a debugging

session" will not be further examined on the merits.

Claims 2-8:

These claims are also rejected because they depend on claim 1 and have the

same problems of failing to comply with the enablement requirement.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

5.   Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shen

et al. (US-6829751), hereinafter Shen.

Claim 1:

Shen teaches a standard cell, the standard cell (Fig. 2, circuit 102) including a

plurality of logic functions (Fig. 2, circuit 110, 112, 114); at least one bus coupled to at

least a portion of the logic functions; a plurality of internal signals from the plurality of

logic functions (Fig. 2, bus and internal signals 140, 142, 144, 146); and a field

programmable gate array (FPGA) function (Fig. 2, FPGA Core) coupled to the at least

one bus (Fig. 2, bus 140, 142, 144, 146, 152) and the plurality of internal signals, the

FPGA function including a debug client function that observes and manipulates (Col. 2.

ll. 39-44, col. 4, ll. 22-24, col. 5, ll. 1-4, col. 6, ll. 21-25, 45-56) the at least one bus and

the plurality of internal signals. (Col. 2, l. 39 to col. 6, l. 65). Shen teaches storage logic

operable to store a state of the selected ones of the plurality of internal signals that

match the trigger pattern for later retrieval by the network server. (Fig. 2, chip registers

120*a*-120*n* and 122*a*-122*n*, Col. 3, ll. 37-41, col. 4, ll. 34-58, col. 5, ll. 36-41).

Shen does not explicitly teach "comparator logic operable to compare selected

ones of a plurality of internal signals coupled to the FPGA core with a trigger pattern

downloaded from a network server". However, Shen does teach monitoring the

correctness of a bus protocol (Col. 6, l. 14), that the FPGA core 116 can also be used to

add or verify bug fixes (Col. 6, ll. 52-54), and in claim 1, is configured to detect errors

when in a first mode and verifies fixes of errors in said functional portion. It would have

been obvious to one of ordinary skill in the art at the time the invention was made to that

Shen possesses the claimed comparator logic. The artisan would be motivated to do so

because the functions of monitoring, verifying bug fixes, and detecting errors cannot be

accomplished without "comparator logic operable to compare selected ones of a

plurality of internal signals coupled to the FPGA core with a trigger pattern downloaded

from a server (expected values)". The artisan would also be motivated to do so because

in order to verify or detect errors one of ordinary skill in the art must compare (i.e.

comparator logic) a result to a known good or expected value.

Claim 2:

Shen teaches at least one bus comprises an internal bus (Fig. 2, buses 140, 142,

144, 146).

Claim 3:

Shen teaches the server comprises a network server running a debugger

application. (Col. 5, ll. 13-25, 41-45, col. 6, ll. 1-17).

Claims 4:

Shen teaches debug client function (FPGA Core 116) is programmed by the

network server (Debugging Workstation 104). (Col. 3, ll. 49-54).

Claim 5:

Shen teaches "the debug client function (FPGA core 116) further includes an

external communicator logic function for receiving and transmitting information to a

server (Debugging Workstation 104)" (Col. 3, ll. 25-26, col. 5, ll. 13-20), and "selector

logic coupled to the at least one bus and the plurality of internal signals...", (Fig. 2, mux

134, Col. 3, l. 58 to col. 4, l. 3). Shen also teaches "an interface logic coupled between

the external communicator logic and the selector logic for providing communication

there between" in that there is circuitry within the FPGA core 116 programmed by the

Debugging Workstation 104 (Col. 5, 13-25) to execute debugging diagnostics, some of

which are outlined in col. 6, ll. 1-57.

Claim 6:

Shen teaches that the interface logic comprises of a storage logic function for storing a state of signals of interest from the selector logic and providing the state to a server (on chip registers, col. 5, ll. 36-39), a comparator logic function coupled to the storage logic function for comparing the signals of interest from the selector block function (Col. 5, ll. 39-45, col. 6, ll. 32-44), and an output logic function coupled to the comparator logic function for controlling the internal signals on the ASIC (Col. 3, ll. 22-27, ll. 49-54).

Claim 7:

Shen teaches the server utilizes the debug client to debug hardware within at least one of the plurality of logic functions. (Col. 2, ll. 42-45, Fig. 2).

Claim 8:

Shen teaches the server utilizes the debug client to debug software within at least one of the plurality of logic functions. (Col. 6, ll. 1-63).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN J. TABONE JR whose telephone number is (571)272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, JACQUES H. LOUIS JACQUES can be reached on (571) 272-6962. The

fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/John J. Tabone, Jr./
Examiner
Art Unit 2117   10/9/2008